

FORM PTO-1390 (Modified)
(REV 11-2000)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

BERGLUNDS P9918

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR

10/009326

INTERNATIONAL APPLICATION NO.

PCT/SE00/01134

INTERNATIONAL FILING DATE

31 May 2000 (31.05.00)

PRIORITY DATE CLAIMED

4 June 1999 (04.06.1999)

TITLE OF INVENTION

LOW-POWER SENSOR

APPLICANT(S) FOR DO/EO/US

DANICK, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
 - a. ☒ is attached hereto (required only if not communicated by the International Bureau).
 - b. ☐ has been communicated by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
 - a. ☐ is attached hereto.
 - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
 - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
 - b. ☐ have been communicated by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☒ have not been made and will not be made.
8. ☒ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information: Submission of Incomplete Application

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR

INTERNATIONAL APPLICATION NO.

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24. The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

- ☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **\$1040.00**
- ☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **\$890.00**
- ☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **\$740.00**
- ☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **\$710.00**
- ☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **\$100.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =**\$1,040.00**Surcharge of **\$130.00** for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492 (e)). ☐ 20 ☐ 30**\$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE
Total claims	26 - 20 =	6	x \$18.00
Independent claims	1 - 3 =	0	x \$84.00

\$108.00**\$0.00**Multiple Dependent Claims (check if applicable). ☐**\$0.00****TOTAL OF ABOVE CALCULATIONS =****\$1,148.00**

- ☒ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.

\$574.00**SUBTOTAL =****\$574.00**Processing fee of **\$130.00** for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492 (f)). ☐ 20 ☐ 30 +**\$0.00****TOTAL NATIONAL FEE =****\$574.00**Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). ☐**\$0.00****TOTAL FEES ENCLOSED =****\$574.00**

Amount to be:	\$
refunded	
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- a. ☐ A check in the amount of _____ to cover the above fees is enclosed.
- b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.
- c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **08-1391**. A duplicate copy of this sheet is enclosed.
- d. ☒ Fees are to be charged to a credit card. **WARNING: Information on this form may become public. Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

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Reg. No. 24,315

REGISTRATION NUMBER

December 4, 2001

DATE

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10/009326

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln Of: DANICK, et al.
Serial No.: December 4, 2001
Filed:
For: LOW-POWER SENSOR

DOCKET: BERGLUNDS P9918

The Assistant Commissioner of Patents
Washington, D.C., 20231

PRELIMINARY AMENDMENT

Dear Sir:

Applicant respectfully requests that you make the following amendment prior to examination.

IN THE CLAIMS:

Please amend claims 4-6, 8-11, 17-20, 22, 23 and 26 to read as follows:

4. (Amended) A micro-hotplate device according to claim 1, wherein at least one temperature-sensing element is a temperature-sensitive resistor.

5. (Amended) A micro-hotplate device according to claim 1, wherein at least one temperature-sensing element is a temperature-sensitive diode.

6. (Amended) A micro-hotplate device according to claim 1, wherein said membrane consists of one or several insulator layers.

8. (Amended) A micro-hotplate device according to claim 6, wherein electrically conducting leads to the active microelectronic devices on the island have been placed between different insulator layers.

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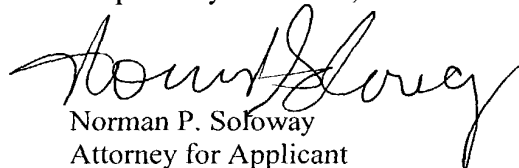
REMARKS

The claims have been amended to remove multiple dependencies. The Applicant requests that the filing fee be calculated based on the claims as amended. Examination of the application, as amended, is respectfully requested.

Pursuant to 35 CFR 1.121, a marked copy of the amended claims showing changes made therein accompanies this amendment.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,



Norman P. Sofoway
Attorney for Applicant
Reg. No. 24,315

CERTIFICATE OF EXPRESS MAILING

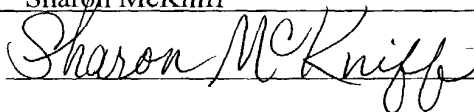
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Date of Deposit December 4, 2001

I hereby certify that this paper and the papers listed thereon are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, and is addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231.

Name of person mailing Sharon McKniff

Signature of person mailing



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MARKED COPY OF AMENDED CLAIMS:

4. (Amended) A micro-hotplate device according to [any of the claims 1-3] claim 1, wherein at least one temperature-sensing element is a temperature-sensitive resistor.

5. (Amended) A micro-hotplate device according to [any of the claims 1-3] claim 1, wherein at least one temperature-sensing element is a temperature-sensitive diode.

6. (Amended) A micro-hotplate device according to [any of the claims 1-5] claim 1, wherein said membrane consists of one or several insulator layers.

8. (Amended) A micro-hotplate device according to claim 6 [or 7], wherein electrically conducting leads to the active microelectronic devices on the island have been placed between different insulator layers.

9. (Amended) A micro-hotplate device according to [any of the claims 1-8] claim 1, wherein the semiconducting material in the island is silicon.

10. (Amended) A micro-hotplate device according to [any of the claims 1-8] claim 1, wherein the semiconducting material in the island is silicon carbide.

11. (Amended) A micro-hotplate device according to [any of the claims 1-10] claim 1, wherein the support substrate and the island are made of the same material.

17. (Amended) A method according to [any of the claims 1-16] claim 12, wherein at least one of said etching steps is an anisotropic potassium hydroxide etching step.

18. (Amended) A method according to [any of the claims 12-16] claim 12, wherein at least one of said etching steps is an anisotropic tetramethyl ammonium hydroxide etching step.

19. (Amended) A method according to [any of the claims 12-16] claim 12, wherein at least one of said etching steps is a deep reactive ion etching step.

20. (Amended) A micro-hotplate device according to [any of the claims 1-12] claim 1, wherein one or several of the chemical sensors utilize the field-effect detection mechanism.

22. (Amended) A micro-hotplate device according to [any of the claims 1-12 or 21] claim 1, wherein one or several of the chemical sensors are operated as gas sensors.

23. (Amended) A micro-hotplate device according to claim[s] 21[and 22], wherein one or several field-effect gas sensors are combined with one or several gas sensors that utilize resistance changes as detection mechanism.

26. (Amended) A micro-hotplate device according to [any of the claims 1-12 or 20-25] claim 1, wherein the support substrate contains an array of several islands.

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LOW-POWER SENSOR
INTRODUCTION

Gas-sensitive field-effect (GasFETs) devices have been studied for about 25 years. The replacement of the MOSFET gate by materials having catalytic properties (Pt, Pd, Ir...) allows the detection of several gases. During the years, they have shown to be suitable for different applications such as hydrogen monitor and leak detectors and electronic noses. Portable instruments and automotive industry are markets where low-cost and low-power consumption devices are in constant development. During the last years, a lot of work has been done in the gas sensing field on reducing the power consumption of resistive gas sensors devices, but none has been reported on MOSFET type gas sensors. They are when used usually heated to a temperature over 100 °C to increase sensitivity and are limited to 175-200°C due to the use of standard silicon fabrication technologies. The present power consumption for one sensor is about 0.5 to 1.0 W, a major part of which is used to heat the sensor to its working temperature. A low-power consumption array of GasFETs has been developed to make this technology competitive with the others on these markets.

In view of said comparatively high power consumption it is the object of the invention to lower this for gas-sensitive field-effect (GasFETs) devices.

THE INVENTION

The object of the invention is solved by means of a design and fabrication methodology for micro-machined semiconductor devices comprising "hotplate devices", which makes it possible to combine micro-machining processing with the integration on the hotplate of active microelectronic chemical sensors exposed to the ambient. The device includes a support substrate, a membrane extending over a well in the substrate, and a semiconductor island attached to the membrane and isolated thermally, from the support substrate. The semiconductor island serves as a substrate for the integration of microelectronic chemical sensors, which are exposed to the ambient for instance through a hole in the membrane. The device may include also other active microelectronic components, e.g., circuits for control and sensing, which may be protected by the membrane if required. By including an electric heater and a temperature sensor in the island, a micro-hotplate chemical sensor device is obtained that can be heated under temperature control using very low power. The most important advantage of the disclosed device as compared to traditional devices is that any active microelectronic chemical sensor can be integrated in the hotplate, while still being exposed to the ambient gas or liquid surrounding the device. With the

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disclosed device, it becomes possible to utilize chemical sensors based on the so-called field-effect detection mechanism. Field-effect gas sensors have proven to be very useful in many applications, either as single sensors, as arrays consisting of several sensors, or in combination with one or several sensors that utilize a different detection mechanism. By utilizing the disclosed device, it becomes possible to make low-power field-effect gas sensors and sensor arrays. Due to the low thermal mass of the disclosed micro-hotplate devices, the operating temperature of the field-effect gas sensors can be pulsed or varied swiftly in some other way and sensors integrated in the same micro hotplate can be operated at different temperatures. Arrays of multiple sensors can be integrated on the disclosed micro-hotplate together with individual circuits for control and sensing, allowing an independent operation of each individual sensor. Also heating to operating temperatures can be very quick, almost instantaneous. The resulting devices are, e.g., suitable for applications in automobiles, portable gas-sensor instruments, and for on-line measurements using distributed sensor systems.

15 EMBODIMENT

Further advantages and developments of the invention are apparent from the claims as well as from the following description of an embodiment with reference to the Fig 1 in the drawings. depicting a cross section of an embodiment of the invention, it should be noted that the cross section is very much enlarged and not to scale since the dimensions in the vertical direction (as viewed) is enlarged many times more than the horizontal direction for improved illustration. Fig 2 shows a similar device somewhat simplified and fabricated in accordance with claim 13. Fig 3 illustrates yet another way to fabricate a micro-hotplate, this time in accordance with claim 15. In fig 4 a micro-hotplate made in accordance with claim 16 is shown. Fig. 5 is a cross section of a device similar to fig 1, but where the sensor is contactable by for instance ambient gas in a more direct manner.

Sensor chip

The MOSFETs array gas sensor realized (fig. 1) has been designed in the aim of reducing the source and drain leakage currents and the power consumption of this type of gas sensors. Each device consists of 4 GasFETs, a temperature sensor (diode) and a heater. The actual chip size is 4.0 x 4.0 mm².

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Electronic components

The heater is a semiconducting resistor, which is made during the p-well implantation of the MOSFET fabrication process. The transistors (NMOS) and the diode temperature sensor are made in a single diffusion step of doping atoms from CVD oxide films. Arrays with 4 medium or small MOSFETs have been designed respectively with a channel length of 13.0 and 5.0 μm . The fabrication of NMOS transistors in a p-well technology allows to drive them separately. Their source/drain leakage currents have been limited by minimizing the p-n junction surface at the source and the drain regions. Therefore, the metal / semiconductor contacts are directly taken on the source and the drain just beside the gate. GasFETs operate with their drain and gate connected together with a constant current bias between the source and the drain. In this design, the drain and gate were not connected together to allow more flexibility during the characterization of the MOSFETs electrical properties.

Power consumption

The thermal mass and therefore the power consumption of the sensor are minimized by the design. The GasFETs, the heater and the diode are located in a silicon island isolated from the chip frame by a dielectric membrane. The membrane is made of LPCVD low-stress silicon nitride. A PECVD silicon nitride film is used as a passivation layer on the aluminum metallization. The membrane size is $1.8 \times 1.8 \text{ mm}^2$ and the silicon island area is $900 \times 900 \mu\text{m}^2$ and 10 μm thick.

FABRICATION

Three main parts compose the fabrication process:

25

1. Fabrication of the doped regions in the silicon to make the electronic components;
2. Gate oxide growth and deposition of the membrane, the metallization, and passivation films; and
3. Release of the membrane and the formation of the silicon island by for instance wet anisotropic etching of silicon.

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Electronic components

The process starts with the implantation of boron in a 4" silicon substrate (25 Ωcm , n type).

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300 μm thick double face polished) to form the MOSFETs p-well, the p side of the diode and the resistive heater. Also included in this first part is the deposition and patterning of boron and phosphorus doped CVD oxide films and the diffusion of the doping atoms to form the n+ and p+ regions of the electronic devices.

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Membrane, metallization and passivation

The second part starts with the growth of a thermally gate oxide (100 nm) followed by the deposition of a low-stress silicon rich nitride LCPVD film. Then, the gate and contacts are defined in the nitride. The metallization is deposited by e-beam evaporation of aluminum, which is annealed to form ohmic contacts on silicon. A PECVD reactor is used to deposit a silicon nitride passivation layer on the device. After the patterning of the passivation film, thin catalytic metals (CM : Pt, Ir, Pd) are deposited, patterned and annealed. GasFETs with 4 different catalytic metals can be fabricated or one of them can be coated by aluminum and used as a reference. Since the deposition of the CM layers is done prior to the bulk silicon micromachining, a chuck is used in the third and last part of the processing to protect the front side of the wafer during the back side etching of silicon in KOH.

15

Silicon bulk micromachining

Firstly, the silicon island is defined and protected by the thermally grown oxide film during the etching of 10 μm of silicon in standard KOH (40% at 60°C) to define the silicon island thickness. Secondly, after the removal of the protective oxide, the silicon is entirely etched by using 52% KOH (solubility limit of KOH in water at room temperature) at 70°C. KOH with a concentration of 52% is used to decrease the etch rate of the (311) planes, forming the side of the silicon island, compared to the etch rate of the (100) plane, which is the plane forming the bottom of the silicon island. The ratio between the etch rates in the direction parallel and perpendicular <100> to the wafer surface is about 1.4 for this specific KOH solution.

25

Despite the fact that the nitride and oxide layers used as membrane are selective to KOH, the release of membrane has to be done with a precise time control of the silicon etching rate to obtain the desired silicon island thickness. Double-face polished wafers with a TTV (Total Thickness Variance) as low as possible are needed since the uniformity of the silicon islands thickness on the entire wafer depends on this parameter.

30

The whole fabrication process includes 50 steps, 15 of which are photolithographies (12 masks). The fabrication process is compatible with the use of different gate insulators as silicon

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dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3) and tantalum oxide (Ta_2O_5).

CHARACTERIZATION

5 Electrical characterizations of MOSFETs designed for this low-power device have shown that they are suitable for gas sensing at temperature up to 225°C . At this maximum operating temperature, a constant current bias of at least $200\text{ }\mu\text{A}$ is needed between the source and drain (connected to the gate) to avoid the interference of leakage currents. Bulk devices coated with thin CM layers (Ir and Pt) show a good sensitivity to H_2 and NH_3 at an operating temperature
10 of 140°C (Fig. 4).

 The heater resistance value is $1175\text{ }\Omega \pm 30\%$ and decreases as a function of temperature with the behaviour expected for a semiconductor. Power consumption of the device has been evaluated by using the diode previously calibrated as a function of temperature. A low power consumption of 80 mW is achieved for an operating temperature of 175°C for the array of 4
15 GasFETs compared to $0.5\text{--}1.0\text{ W}$ for one standard GasFET

 The silicon island ensures a uniform temperature distribution all over the active area. The low thermal mass allows the operation of the sensor in a temperature cycling mode, which enhances the power consumption of the device and could influence the selectivity as in resistive gas sensors.

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CONCLUSIONS

 The design, fabrication and characterization of a low-power consumption MOSFETs array gas sensor have been presented. The sensor consists of a heating resistor, a diode temperature sensor and 4 GasFETs located in a silicon island thermally isolated from the chip frame by a
25 dielectric membrane. The combination of microelectronics and MEMS (silicon bulk micro-machining) fabrication technologies was used to fabricate these devices. The array of 4 GasFETs has a low-power consumption of 80 mW at an operating temperature of 175°C . The silicon island also provides a uniform temperature all over the sensing area. The low thermal mass of the device allows the operation of the sensors in a temperature cycling mode.

30 Even if above and in the drawings the island has been described and shown without semiconductor (for instance) silicon in the membrane connection with the support, the membrane may comprise silicon without loss of thermal isolation. The silicon in the membrane may be thin, shaped as spokes or low-doped or even undoped or combinations thereof rendering the thermal

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losses through the silicon small.

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Claims

1. Micro-hotplate device with integrated chemical sensor, which comprises:

- a) a support substrate;
- b) a supported membrane, attached to said support substrate, extending over a well in said support substrate;
- c) an island attached to said membrane so as to be electrically and thermally isolated from said substrate, said island consisting at least partly of a semiconducting material;
- d) one or several heating elements integrated in said island;
- e) one or several temperature-sensing elements integrated in said island;
- f) one or several active microelectronic devices integrated in said island, where at least one of said active microelectronic devices is a gas-sensitive field-effect sensor whose chemically active layer is exposed to the ambient.

2. A micro-hotplate device according to claim 1, wherein at least one heating element consists of a heating transistor.

3. A micro-hotplate device according to claim 1, wherein at least one heating element consists of a heating resistor.

4. A micro-hotplate device according to any of the claims 1-3, wherein at least one temperature-sensing element is a temperature-sensitive resistor.

5. A micro-hotplate device according to any of the claims 1-3, wherein at least one temperature-sensing element is a temperature-sensitive diode.

6. A micro-hotplate device according to any of the claims 1-5, wherein said membrane consists of one or several insulator layers.

7. A micro-hotplate device according to claim 6, wherein at least one insulator is silicon nitride.

8. A micro-hotplate device according to claim 6 or 7, wherein electrically conducting leads to the active microelectronic devices on the island have been placed between different insulator layers.

9. A micro-hotplate device according to any of the claims 1-8, wherein the semiconducting material in the island is silicon.

10. A micro-hotplate device according to any of the claims 1-8, wherein the semiconducting material in the island is silicon carbide.

11. A micro-hotplate device according to any of the claims 1-10, wherein the support

steps is an anisotropic tetramethyl ammonium hydroxide etching step.

19. A method according to any of the claims 12-16, at least one of said etching steps is a deep reactive ion etching step.

20. A micro-hotplate device according to any of the claims 1-12, wherein one or several of
5 the chemical sensors utilize the field-effect detection mechanism.

21. A micro-hotplate device according to claim 20, wherein one or several field-effect chemical sensors are combined with one or several chemical sensors that utilize a detection mechanism different from the field effect.

22. A micro-hotplate device according to any of the claims 1-12 or 21, wherein one or
10 several of the chemical sensors are operated as gas sensors.

23. A micro-hotplate device according to claims 21 and 22, wherein one or several field-effect gas sensors are combined with one or several gas sensors that utilize resistance changes as detection mechanism.

24. A micro-hotplate device according to claim 23, wherein at least one of the gas sensors
15 that utilize resistance changes as detection mechanism is made of a semiconducting metal oxide.

25. A micro-hotplate device according to claim 23, wherein at least one of the gas sensors that utilize resistance changes as detection mechanism is made of a polymer.

26. A micro-hotplate device according to any of the claims 1-12 or 20-25, wherein the support substrate contains an array of several islands.

27. A micro-hotplate device according to any of the claims 1-12 or 20-26, wherein the
20 sensor is exposed to the ambient through a hole in the membrane.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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14 December 2000 (14.12.2000)

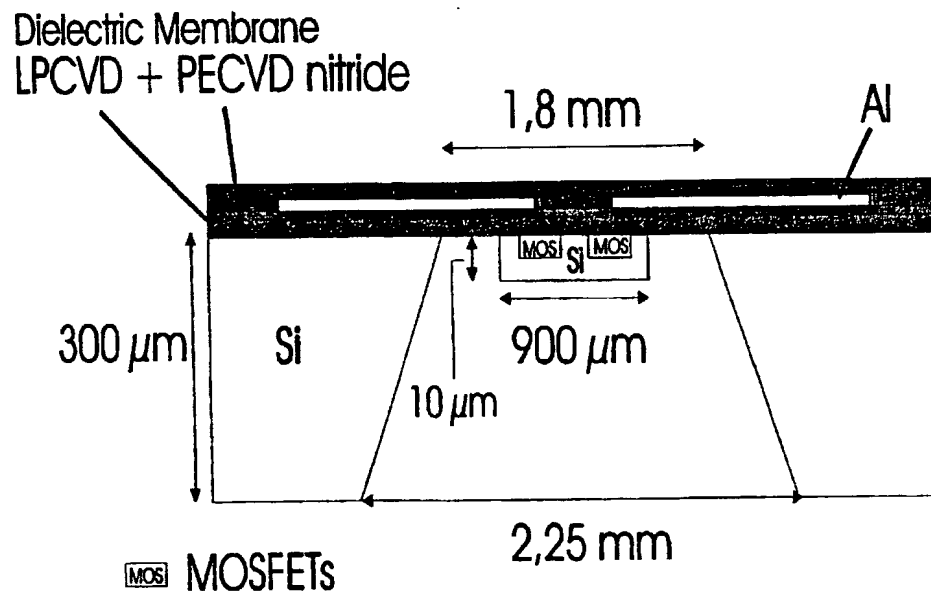
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BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK,
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LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT,
RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA,
UG, US, UZ, VN, YU, ZA, ZW.**(84) Designated States (regional): **ARIPO patent (GH, GM,
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patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European**

[Continued on next page]

(54) Title: **LOW-POWER SENSOR**

(57) Abstract: The invented MOSFET array gas sensor has been fabricated using silicon bulk micro machining. A heating resistor, a diode used as temperature sensor and 4 gas-sensitive FETs are located in a silicon island suspended by a dielectric membrane. The membrane has a low thermal conductivity coefficient and therefore thermally isolates the electronic components on the silicon island from the chip frame. This low thermal mass device allows the reduction of the power consumption to a value of 80 mW for an operating temperature of 175 °C. This low power MOSFETs gas sensor array is suitable for applications in portable gas sensors instruments and in automobiles.

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patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:

— *With international search report.*

— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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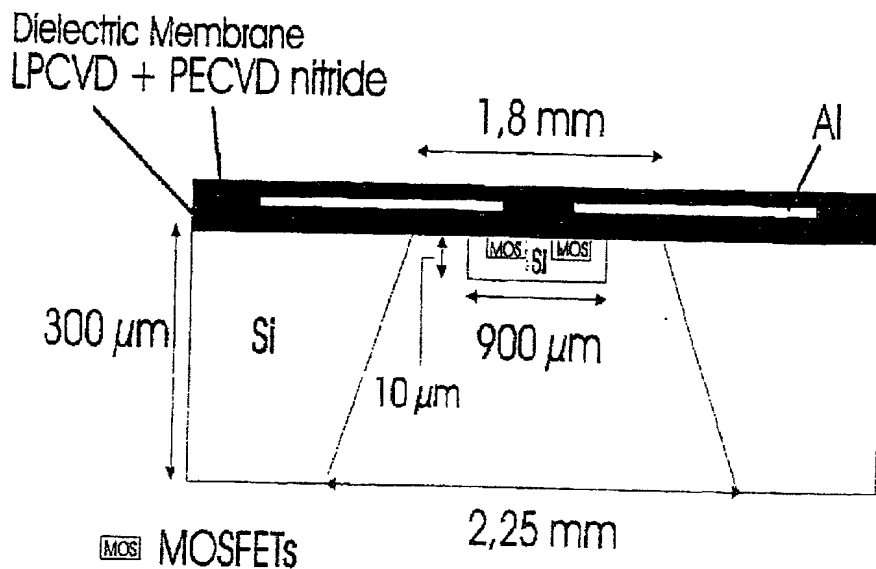


Fig 1

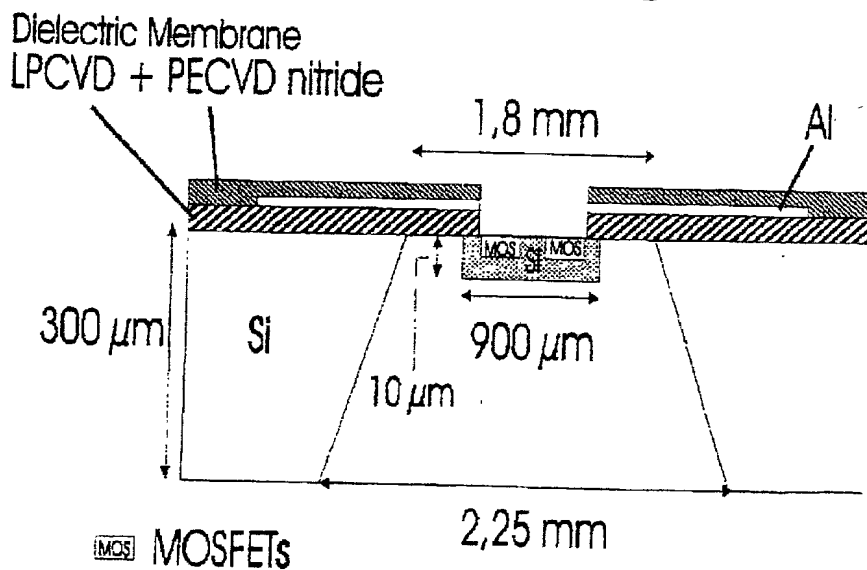


Fig 5

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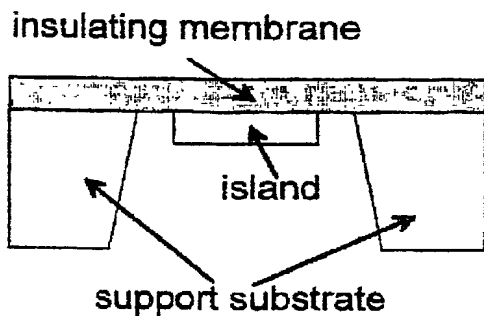


Fig 2

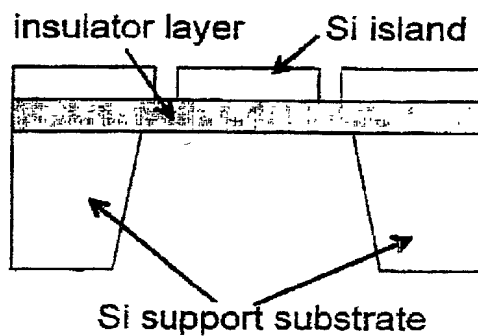


Fig 3

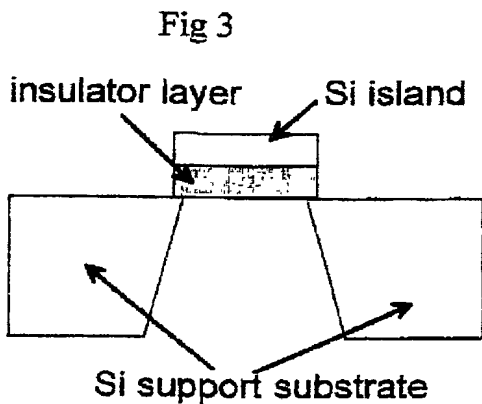
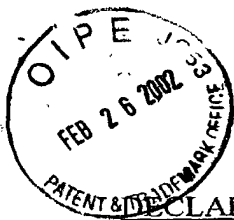


Fig 4



10009326-022502

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No: _____

First Named Inventor: Briand Danick

Complete if known: Serial No: _____ Filing Date: _____

Group Art Unit: _____ Examiner: _____

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Low-power sensor

_____, the
specification of which: ☐ is attached hereto or ☐ was filed on _____ as
application Serial No. _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, S. 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

<u>9902081-0</u>	<u>Sweden</u>	<u>June/04/1999</u>	<u>Priority Claimed</u>	<u>Certified Copy Attached</u>
(Number)	(Country)	(Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	<input type="checkbox"/> Yes <input type="checkbox"/> No
_____	_____	_____	<input type="checkbox"/> Yes <input type="checkbox"/> No	<input type="checkbox"/> Yes <input type="checkbox"/> No
(Number)	(Country)	(Month/Day/Year Filed)		

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below:

Application No: _____ Filing Date: _____

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

<u>PCT/SE00/01134</u>	<u>May/31/2000</u>	<u>PCT/SE00/01134</u>
US Parent Application or PCT Parent Number	Parent Filing Date	Parent Patent Number (if applicable)

And I hereby appoint HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., a firm composed of Oliver W. Hayes, Reg. No. 15,867; Norman P. Soloway, Reg. No. 24,315; William O. Hennessey, Reg. No. 32,032; Susan H. Hage, Reg. No. 29,646; Steven J. Grossman, Reg. No. 35,001; Christopher K. Gagne, Reg. No. 36,142; and Edmund Paul Pfleger, Reg. No. 41,252, or any of them, of 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith.

Please direct all future correspondence in connection with this application to the attention of Norman P. Soloway HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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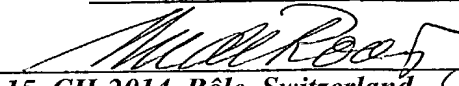
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3-0
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4-0
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5-0
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Full name of sixth joint inventor: _____

Sixth Inventor's signature _____ Date _____
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[illegible]

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Fourth Inventor's signature *[Signature]* Date 7/12 - 2001

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Fifth Inventor's signature [Signature] Date 5/12/2000

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Full name of sixth joint inventor: _____

Sixth Inventor's signature _____ Date _____

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